

REMARKS

Claims 17-21 are pending in the application. In the Office Action of July 7, 2004, the Examiner made the following disposition:

- A.) Objected to the specification.
- B.) Rejected claims 17-18 and 20-21 under 35 U.S.C. §102(e) as being anticipated by *Eichelberger*.
- C.) Rejected claim 19 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Gates*.

Applicants respectfully traverse the rejections and addresses the Examiner's disposition below.

A.) Objection to the specification:

The Examiner objected to the title of the invention. The title of the invention has been amended as per the Examiner's request to overcome the objection.

The Examiner objected to the specification as allegedly not providing antecedent basis for claim 19. Claim 19 has been amended as per the Examiner's request to overcome the objection.

Applicants respectfully submit the objections have been overcome and request that they be withdrawn.

B.) Rejection of claims 17-18 and 20-21 under 35 U.S.C. §102(e) as being anticipated by *Eichelberger*:

Applicants respectfully disagree with the rejection.

Independent claim 17, as amended, claims a method of fabrication of a semiconductor device. A plurality of semiconductor chips are die bonded on a substrate. A single-layer insulation film is formed on the substrate, wherein a top surface and at least a portion of side surfaces of the plurality of semiconductor chips are is incrustated in the insulation film. A connection hole is formed reaching a semiconductor chip of the plurality of semiconductor chips on the insulation film. Wiring is formed on the insulation film, wherein the wiring is connected to the semiconductor chip through the connection hole.

Thus, Applicants' claimed semiconductor device is easy to manufacture, since its requires formation of a single-layer insulation film, instead of a multi-layered insulation film.

This is clearly unlike *Eichelberger*, which fails to disclose or even suggest forming a single-layer insulation layer that encrusts a top surface and at least a portion of side surfaces of a plurality of chips. Referring to *Eichelberger* Figure 5g, *Eichelberger* discloses encasing the sides of a chip 102 in a structure material 104 and then covering the top of the chip with a first dielectric layer 106. As clearly shown in Figure 5g, unlike Applicants' claim 7, *Eichelberger's* chip's top and sides are clearly not encrusted in a single-layer insulation layer. Instead, the sides of *Eichelberger's* chip are encrusted in the structure material 104, and the top of *Eichelberger's* chip is covered by the first dielectric layer 106. The first dielectric layer 106 does not encrust the sides of *Eichelberger's* chip.

Therefore, *Eichelberger* fails to disclose or even suggest Applicants' claim 17.

Claims 1 and 20-21 depend directly or indirectly from claim 17 and are therefore allowable for at least the same reasons that claim 17 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claim 19 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Gates*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 17 is allowable over *Eichelberger* as discussed above. *Gates* still fails to disclose or suggest forming a single-layer insulation layer that encrusts a top surface and at least a portion of side surfaces of a plurality of chips. Therefore, *Eichelberger* in view of *Gates* still fails to disclose or suggest Applicants' claim 17.

Claim 19 depends directly or indirectly from claim 17 and is therefore allowable for at least the same reasons that claim 17 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 17-21 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on October 20, 2004.

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